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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,027	07/30/2001	David R. Maciorowski	10018842-1	1027

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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,027	MACIOROWSKI ET AL.	
	Examin r	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Submission of Application dated 7/30/2001.

2. Claims 1-20 are presented for examination.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It was not executed (signed) in accordance with either 37 CFR 1.66 or 1.68.

A letter was received on 12/27/01 with reference to an executed oath/declaration, but there was no copy of an executed oath/declaration.

Claim Objections

4. Claims 1 and 16 are objected to because of the following informalities:

a. Regarding claim 1, on line 19 of the claim, "module" should be changed to "controller" to avoid lack of antecedent basis.

b. Regarding claim 16, on line 4 of the claim, "the group" should be changed to "a group" to prevent a lack of antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Blake et al, U.S. Patent 6,528,987 and Garcia et al., 6,151,689.

7. Regarding claim 1, AAPA teaches a backup management system for providing basic system functions in a computer system, comprising:

a. a plurality of system sensors for detecting power and temperature in the computer system (paragraph 2);

b. a management processor, coupled to said sensors (it is inherent that in order to monitor power and temperature sensors must be coupled to the management processor, paragraph 2);

c. a high-availability controller (backup management processor), operably coupled to said management processor and to said sensors (in operating as a backup management processor it is necessary that it is operably coupled to the sensors and to the management processors in order to determine if the management processor is unable to function, paragraph 3);

d. a management processor status signal generated to indicated an operational state thereof, and coupled to said high availability controller (necessary in order for the backup management processor to act in place for the management processor, paragraph 3);

e. wherein said sensors include:

i. a plurality of power controllers (inherent for control of power and power sequencing), each of which monitors the state of an associated power supply in the computer system and controls power thereto (paragraph 2);

f. wherein during normal operation of the computer system, said management processor monitors outputs from said sensors and sends control signals to said power controllers (it would follow that during normal operations that the management processor would monitor and control as its operation is to do such, paragraph 2); and

g. wherein, in response to detecting that said management processor status signal is inactive (inherent in order to detect management processor is unable to function), said high availability controller (backup management processor) generates control signal in response to outputs from said sensors to control operation of said power controllers (it would also follow as a backup management processor, that the duties of the management processor would be executed by the backup management processor upon detecting the management processor is unable to carry out processing, paragraph 3).

AAPA does not disclose a sensor for detecting cooling fan speed in the computer system, wherein said sensors include at least one cooling fan controller for detecting and controlling said cooling fan speed, and wherein the management processor and the high availability controller control operation of said fan controller. AAPA must generate a processor management signal but also does not disclose that said management processor generates the management processor status signal.

Blake teaches a sensor for detecting cooling fan speed in computer system wherein said sensors include at least one cooling fan controller for detecting and controlling the fan speed (col. 4 lines 14-34 and col. 6 lines 28-32). Blake also teaches a management processor to control the cooling fan and used in a system similar to that of AAPA. Blake teaches controlling the cooling fan has many advantages such as reducing failure and destruction of components within the computer cabinetry (col. 1 lines 43-52). Further advantages are taught in Blake at beginning at col. 4, line 31.

It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Blake before them at the time the invention was made, to modify the management processor of AAPA to include control of a cooling fan as taught by Blake in order to control the temperature of the system.

One of ordinary skill in the art would have been motivated to make this modification in order to reduce the chance of failure and destruction of components with the computer cabinetry in view of the teachings of Blake. In making this modification it would follow that the management processor would monitor outputs of the cooling fan controller as well.

Garcia teaches management processor that generates a management processor status signal ("I'm alive" signal). The system of Garcia is similar to that of AAPA in that Garcia further teaches that when the management processor signal is inactive a high a high availability controller (backup processor) that assumes the tasks of controlling components when the management processor fails (col. 3 lines 1-7). Garcia further provides the advantage that the backup processes run by the high availability controller often succeed provide software fault

tolerance since the high availability software environment runs different software to improve reliability of the system (col. 3 lines 8-18).

It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA and Garcia before them at the time the invention was made, to modify the management processor of AAPA to include the management processor status signal as taught by Garcia in order to obtain a fault tolerant system.

One of ordinary skill in the art would have been motivated to make the modification in order to improve reliability of the system in view of the teachings of Garcia.

8. Regarding claim 6, AAPA together with Blake and Garcia taught the backup management system according to claim 1 as described above. Garcia teaches wherein said management processor includes a watchdog timer that sets the management processor status signal ("I'm alive" message) to an inactive state when the management processor does not reset the timer within a predetermined period of time (col. 2 lines 55-67). Garcia discloses periodically broadcasting an "I'm alive" message, which must entail resetting a timer within a predetermined period of time. The message is sent when a processor is alive and the message is not sent the processor does not reset timer. Even if AAPA, Blake and Garcia do not disclose wherein said management processor includes a watchdog timer that sets the management processor status signal to an inactive state when the management processor does not reset the timer within a predetermined period of time it would have been obvious to one of ordinary skill in the art to implement a watchdog timer to do. Watchdog timers are well know in the art and are used to determine if a processor has failed. In using a watchdog timer, if a processor fails to act within a predetermined time period a message will be sent to notify other circuitry that the

processor has failed. One of ordinary skill in the art would have been motivated to use a watchdog timer in order to determine if a processor has failed because they are often used for such function and are highly reliable and can be set to provide variable time at which failure is determined.

9. Regarding claim 7, AAPA together with Blake and Garcia teach the backup management system according to claim 1 as described above. AAPA further teaches including panel indications coupled and responsive to output signals from the management processor and high availability controller (paragraph 2 and 3). The panel indicators described by AAPA would include front panel indicators as would be known to those of ordinary skill in the art.

10. Claim 2-3, 8, 9, and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA together with Blake and Garcia in view of Tanenbaum, "Structured Computer Organization".

11. Regarding claim 2, AAPA together with Blake and Garcia taught the backup management system according to claim 1, as described above. AAPA together with Blake and Garcia do not disclose teaching including a ***non-software coded state machine*** that monitors said management processor status signal and causes said high availability controller to generated said control signals when said status signal is inactive wherein said state machine performs a different sequence of operations than the code executed by said management processor [emphasis added].

Specifically, Garcia appears to teach a ***software coded state machine*** that monitors said management processor status signal and causes said high availability controller to generated said control signals when said status signal is inactive and wherein said state machine performs a

different sequence of operation that the code executed by said management processor (backup processor) [emphasis added].

Tanenbaum teaches that hardware and software are logically equivalent, that is, any operation performed by software can be built directly into hardware and any instruction executed in hardware can be simulated in software (page 11, specifically 1-4 full paragraphs on the page). Tanenbaum further teaches that the implementation is dependent upon the goal of the designer. Tanenbaum teaches that constructing a non-software coded state machine (implementation hardware circuits) is desirable to enable faster execution of the state machine.

It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Blake, Garcia and Tanenbaum before them at the time the invention was made, to implement the state machine that monitors the management processor status signal of the combination of AAPA, Blake, and Garcia as a non-software coded state machine as taught by Tanenbaum.

One of ordinary skill in the art would have been motivated to make this modification in order to make the state machine faster in view of the teachings of Tanenbaum.

12. Regarding claim 3, AAPA together with Blake, Garcia, and Tanenbaum teach the backup management system according to claim 2, as described above. The combination does not disclose wherein said state machine is a field programmable gate array.

The examiner takes official notice of field programmable gate arrays. Field programmable gate arrays are well known by those of ordinary skill in the art as hardware devices used to implement a function without running software. Furthermore, field

programmable gate arrays are, as the name suggest, programmable by a user and thus have the advantage of being able to change functionality of the hardware when desired.

It would have been obvious to one of ordinary skill in the art, having the teachings of AAPA, Blake, Garcia, Tanenbaum and the knowledge of field programmable gate array at the time the invention was made, to implement the backup management system to implement the state machine (backup processor) as taught by AAPA, Garcia and Tanenbaum using a field programmable gate array.

One of ordinary skill in the art would have been motivated to make this modification in order to increase the functionality of the hardware in view of the well known field programmable gate arrays that implement hardware functionality.

13. Regarding claims 8, 9-11 and 14-20, AAPA together with Blake, Garcia and Tanenbaum taught the claimed system, therefore together they also teach the claimed methods.

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claim 1-3, 5-6, 8-9, 11, 14, 16-17 and 19 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1-2, 6-11, and 15-17 of copending Application No. 09/917,984. Although the conflicting claims are not identical, they are not patentably distinct from each other. Below is a table showing why the claims are not patentably distinct.

Instant Application	Application No. 09/917,984
1. A backup management system for providing basic system functions in a computer system, comprising:	1. A multiple redundancy backup management system for providing basic system functions in a computer system, comprising:
a plurality of system sensors for detecting power, temperature, and cooling fan speed in the computer system;	a plurality of system sensors for detecting power, temperature, and cooling fan speed in the computer system;
a management processor, coupled to said sensors;	a plurality of management processors, wherein each of the processors is coupled to each of said sensors;
	wherein a management processor status signal is generated by each of said management processors to indicate an operation state thereof;
a high-availability controller, operably coupled to said management processor and to said sensors;	a high-availability controller, operably coupled to said status signal and to said sensors;
	wherein said high-availability controller comprises a non-software coded state machine that performs a different sequence of operations than the code executed by said management processors;
a management processor status signal, generated by said management processor to indicate an operational state thereof, and coupled to said high-availability controller;	
wherein said sensors include: a plurality of power controllers, each of which monitors the state of an associated power supply in the computer system, and controls power thereto; and at least one cooling fan controller for detecting and controlling said cooling fan speed;	wherein said sensors include: a plurality of power controllers, each of which monitors the state of an associated power supply in the computer system, and controls power thereto; and at least one cooling fan controller for detecting and controlling said cooling fan speed;

wherein, during normal operation of the computer system, said management processor monitors outputs from said sensors and sends control signals to said power controllers and to said fan module; and wherein, in response to detecting that said management processor status signal is inactive, said high-availability controller generates control signals in response to outputs from said sensors to control operation of said power controllers and said fan controller.	and wherein, in response to detecting inactive processor status signals from all said management processors, said high-availability controller generates control signals in response to outputs from said sensors to control operation of said power controllers and said fan controller.
2. The backup management system of claim 1, including a non-software coded state machine that monitors said management processor status signal and causes said high-availability controller to generate said control signals when said status signal is inactive; wherein said state machine performs a different sequence of operations than the code executed by said management processor.	(from above in claim 1) wherein said high-availability controller comprises a non-software coded state machine that performs a different sequence of operations than the code executed by said management processors;

Instant Application	Application No. 09/917,984
3. The backup management system of claim 2, wherein said state machine is a field programmable gate array.	2. The backup management system of claim 1, wherein said state machine is a field programmably gate array.
5. The backup management system of claim 1, further including a power switch, for controlling bulk power to the computer system, coupled to said management processor and said high-availability controller; wherein said high-availability controller is responsive to an output from the power switch to initiate powering down of each said power supply when the management processor has failed.	6. The backup management system of claim 1, further including a power switch, for controlling bulk power to the computer system, coupled to said management processors and said high-availability controller; wherein said high-availability controller is responsive to an output from the power switch to initiate powering down of each said power supply when the management processors have failed.
6. The backup management system of claim 1, wherein said management processor includes a watchdog timer that sets said management processor status signal to an inactive state when the management processor does not reset the timer within a predetermined period of time.	7. The backup management system of claim 1, wherein each of said management processors includes a watchdog timer that sets its said processor status signal to an inactive state when the respective management processor does not reset the timer within a predetermined period of time.
8. A method for backup management of basic	8. A method for multiple redundancy backup

system functions in a computer system, the method comprising the steps of: monitoring, via a management processor, a plurality of sensors for detecting power, temperature, and cooling fan speed in the computer system; generating a processor status signal to indicate an operational state of said management processor; monitoring said processor status signal; and generating, in response to detecting that said processor status signal is inactive, backup control signals, in response to outputs from said sensors, to control operation of said controllers; wherein said backup control signals are generated by a non-software coded state machine, operably coupled to said management processor, said sensors, and said controllers.	management of basic system functions in a computer system, the method comprising the steps of: monitoring, via a plurality of management processors, a plurality of sensors for detecting power, temperature, and cooling fan speed in the computer system; generating a plurality of processor status signals, each signal indicating an operational state of an associated one of said management processors; monitoring said plurality of processor status signals; and generating, in response to detecting that all of said processor status signals are inactive, backup control signals, in response to outputs from said sensors, to control operation of said controllers; wherein said backup control signals are generated by a non-software coded state machine, operably coupled to said management processor, said sensors, and said controllers.
9. The method of claim 8, wherein said state machine performs a different sequence of operations than the code executed by said management processor.	9. The method of claim 8, wherein said state machine performs a different sequence of operations than the code executed by said management processor.
11. The method of claim 8, wherein said sensors include at least one cooling fan controller for detecting and controlling said cooling fan speed, and a plurality of power controllers, each of which monitors the state of, and controls power to, an associated power supply in the computer system, including the step of: sending said control signals and said backup control signals to said power controllers and to said fan module.	10. The method of claim 8, wherein said sensors include at least one cooling fan controller for detecting and controlling said cooling fan speed, and a plurality of power controllers, each of which monitors the state of, and controls power to, an associated power supply in the computer system, including the step of: sending said control signals and said backup control signals to said power controllers and to said fan module.
14. The method of claim 8, including the step of setting a watchdog timer that generates an inactive said processor status signal when the management processor does not reset the timer within a predetermined period of time.	11. The method of claim 8, including the step of setting, for each of said management processors, a watchdog timer that generates an inactive said processor status signal for the associated one of said management processors when the management processor does not reset the timer within a predetermined period of time.
16. A backup management system for providing basic system control functions in a	15. A backup management system for providing basic system control functions in a

computer system comprising: a plurality of system sensors for detecting signals from at least two devices in the group of devices consisting of a power module for monitoring the state of an associated power supply in the computer system, a temperature sensor for monitoring temperature in the computer system, and a cooling fan speed module for detecting and controlling system cooling fan speed; a management processor, coupled to said system sensors; a management processor status signal, generated by said management processor to indicate an operational state thereof; a non-software coded state machine, operably coupled to said management processor and to said system sensors, wherein said state machine performs a different sequence of operations than the code executed by said management processor; wherein, in response to detecting that said status signal is inactive, said state machine generates control signals to said power controllers and to said fan module in response to outputs from said system sensors to control the operation thereof.	computer system comprising: a plurality of system sensors for detecting signals from at least two devices in the group of devices consisting of a power module for monitoring the state of an associated power supply in the computer system, a temperature sensor for monitoring temperature in the computer system, and a cooling fan speed module for detecting and controlling system cooling fan speed; a plurality of management processors, wherein each of the processors is coupled to each of said sensors; wherein a management processor status signal is generated by each of said management processors to indicate an operational state thereof; a non-software coded state machine, operably coupled to each of said management processors and to said system sensors, wherein said state machine performs a different sequence of operations than the code executed by said management processors; wherein, in response to detecting that each said status signal is inactive, said state machine generates control signals to said power controllers and to said fan module in response to outputs from said system sensors to control the operation thereof.
17. The backup management system of claim 16, wherein said controllers include: a plurality of power controllers, each of which monitors the state of an associated power supply in the computer system, and controls power thereto; and at least one cooling fan controller for detecting and controlling said cooling fan speed.	16. The backup management system of claim 15, wherein said controllers include: a plurality of power controllers, each of which monitors the state of an associated power supply in the computer system, and controls power thereto; and at least one cooling fan controller for detecting and controlling said cooling fan speed.
19. The backup management system of claim 16, wherein said management processor includes a watchdog timer that sets said processor status signal to an inactive state when the management processor does not reset the timer within a predetermined period of time.	17. The backup management system of claim 15, wherein each said management processor includes a watchdog timer that sets said processor status signal for the associated processor to an inactive state when the management processor does not reset the timer within a predetermined period of time.

The claims differ in that the present application recites a single management processor while application 09/917,984 recites a plurality of processors. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to increase the number of management processors because a system with a plurality of management processors would allow greater reliability over a system with a single management processor.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

16. Claims 4, and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,823,251 to Giers. This patent teach using redundancy with wherein the backup software is different than the normal operating software.

U.S. Pat. No. 5,984,504 to Doyle et al. This patent teaches a backup control mechanism wherein the backup processor and/or software is different in order to preclude common failures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
January 10, 2005

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SUPERVISORY PATENT EXAMINER
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